

## AMENDMENTS TO THE CLAIMS

Claims 1-19 (cancelled)

Claim 20 (New) A method for fabricating an antifuse structure integrated with a semiconductor device, the method comprising the steps of:

- forming a region of semiconducting material overlying an insulator disposed on a substrate;

- performing an etching process to expose a plurality of corners in the semiconducting material;

- forming a plurality of elongated tips of the semiconducting material at the respective corners by oxidizing the exposed corners to form an oxide thereon and then removing the oxide;

- subsequently forming an oxide layer on the semiconducting material and overlying the corners, the oxide layer having a nominal thickness and a reduced thickness at the corners less than the nominal thickness; and

- forming a layer of conducting material in contact with the oxide layer at the corners, thereby forming a plurality of possible breakdown paths at said corners, between the semiconducting material and the layer of conducting material through the oxide layer.

Claim 21 (New) A method according to claim 20, wherein the region of semiconducting material is a fin formed in a FINFET process.

Claim 22 (New) A method according to claim 20, wherein the region of semiconducting material is a gate region formed in a planar CMOS process.

Claim 23 (New) A method according to claim 21 or claim 22, further comprising the step of doping the region of semiconducting material.

Claim 24 (New) A method according to claim 20, wherein oxidizing the exposed corners is performed in accordance with a low-temperature oxidation process.

Claim 25 (New) A method according to claim 20, wherein the breakdown paths are electrically in parallel.

Claim 26 (New) A method according to claim 20, further comprising the step of applying a voltage to the antifuse structure, thereby converting at least one of the breakdown paths to a conducting path through the oxide layer.

Claim 27 (New) A method according to claim 26, wherein the voltage is applied in accordance with a burn-in process for the device.

Claim 28 (New) A method according to claim 26, wherein the device has a nominal voltage, and the applied voltage is approximately 1.5 times the nominal voltage.

Claim 29 (New) An antifuse structure integrated with a semiconductor device, the structure comprising:

- a region of semiconducting material overlying an insulator disposed on a substrate, the semiconducting material having a plurality of corners with a plurality of elongated tips of the semiconducting material at the respective corners;

- an oxide layer on the semiconducting material and overlying the corners and in contact with the corners, the oxide layer having a nominal thickness and a reduced thickness at the corners less than the nominal thickness; and

- a layer of conducting material in contact with the oxide layer at the corners,

- wherein

- a plurality of possible breakdown paths are disposed at said corners, between the semiconducting material and the layer of conducting material through the reduced thickness of the oxide layer, and

- the elongated tips are formed by oxidation of the exposed corners, the oxide formed thereby being different from the oxide layer.

Claim 30 (New) An antifuse structure according to claim 29, wherein the region of semiconducting material is a fin formed in a FINFET process.

Claim 31 (New) An antifuse structure according to claim 29, wherein the region of semiconducting material is a gate region formed in a planar CMOS process.

Claim 32 (New) An antifuse structure according to claim 29, wherein the region of semiconducting material is a region of doped material.

Claim 33 (New) An antifuse structure according to claim 29, wherein the breakdown paths are electrically in parallel.

Claim 34 (New) An antifuse structure according to claim 29, wherein at least one of the breakdown paths is a conducting path through the oxide layer formed by application of a voltage thereto.

Claim 35 (New) An antifuse structure according to claim 34, wherein the applied voltage is a burn-in voltage for the device.

Claim 36 (New) A method according to claim 34, wherein the device has a nominal voltage, and the applied voltage is approximately 1.5 times the nominal voltage.